FAULT TOLERANT COMPUTER

ABSTRACT

A new method for the detection and correction of environmentally induced functional interrupts (or "hangs") induced in computers or microprocessors caused by external sources of single event upsets (SEU) which propagate into the internal control functions, or circuits, of the microprocessor. This method is named Hardened Core (or H-Core) and is based upon the addition of an environmentally hardened circuit added into the computer system and connected to the microprocessor to provide monitoring and interrupt or reset to the microprocessor when a functional interrupt occurs. The Hardened Core method can be combined with another method for the detection and correction of single bit errors or faults induced in a computer or microprocessor caused by external sources SEUs. This method is named Time-Triple Modular Redundancy (TTMR) and is based upon the idea that very long instruction word (VLIW) style microprocessors provide externally controllable parallel computing elements which can be used to combine time redundant and spatially redundant fault error detection and correction techniques. This method is completed in a single microprocessor, which substitute for the traditional multi-processor redundancy techniques, such as Triple Modular Redundancy (TMR).

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